FIG.1 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION /FETCHING EDGE	SIGNAL SPEED (IN TERMS OF FREQUENCY)
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	f/3
q2	↑ CK2	f/3
q3	↑ CK2	f/4
q4	↑ CK1	f/4
Error1	q2 xor q3	<f/2
Error2	q1 xor q4	<f/2
Ref1	(q3 xor q4)*CK2	<f/2
Ref2	(q3 xor q4)*CK1	<f/2

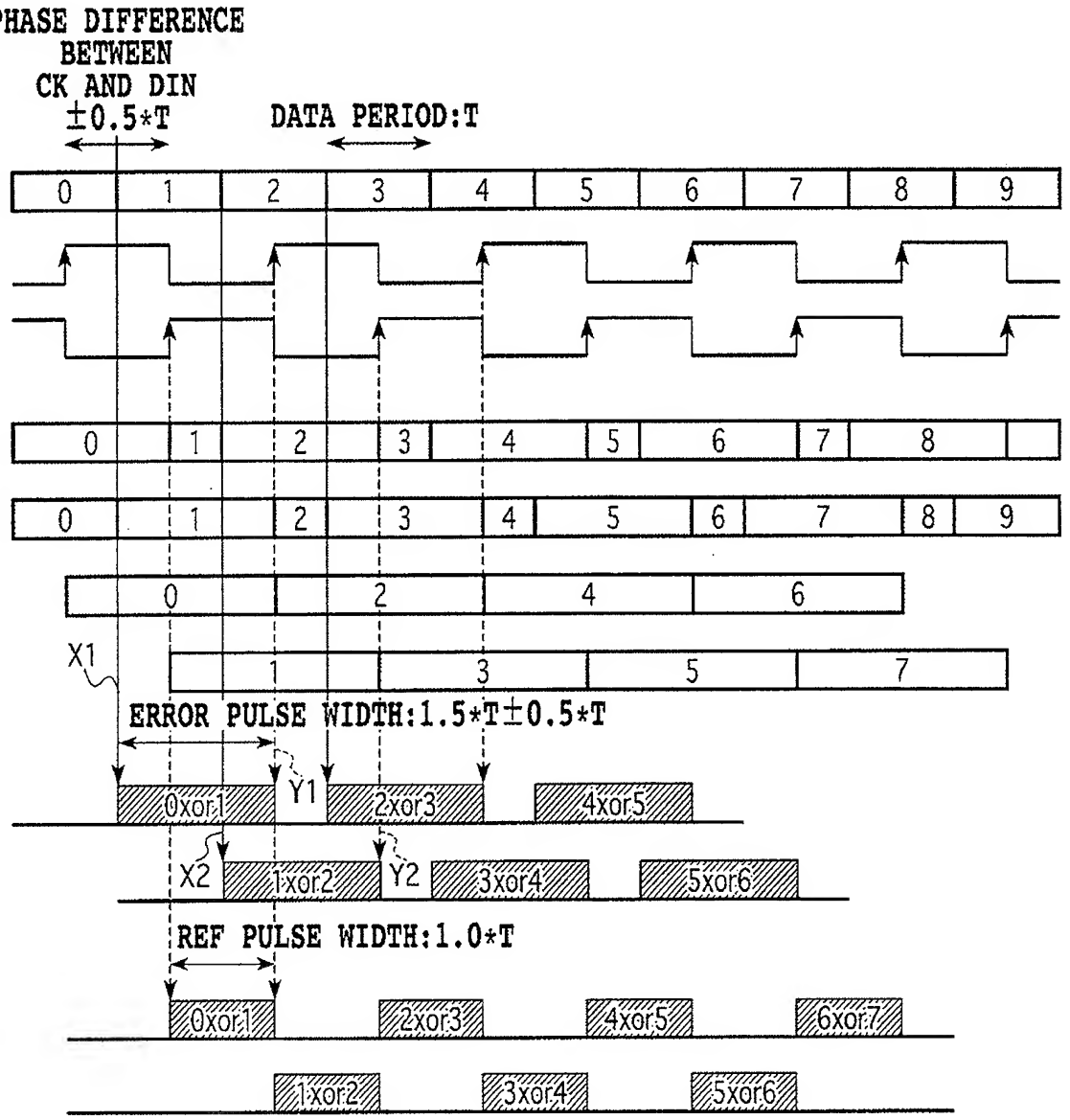

FIG.2 HOLMQVIST AND SUMMERS

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
Input Signal DP		f/2
Reference Clock CK	CK	f/2
	CKN	f/2
D-F/F (31 701 D1	↑ CK	
D-F/F (32 703 D3	↑ CKN	
D-F/F (33 702 D2	↑ CKN	
D-F/F (34 703 D4	↑ CK	
EOR (35 705	D2 xor D3	
EOR (36 706	D1 xor D4	

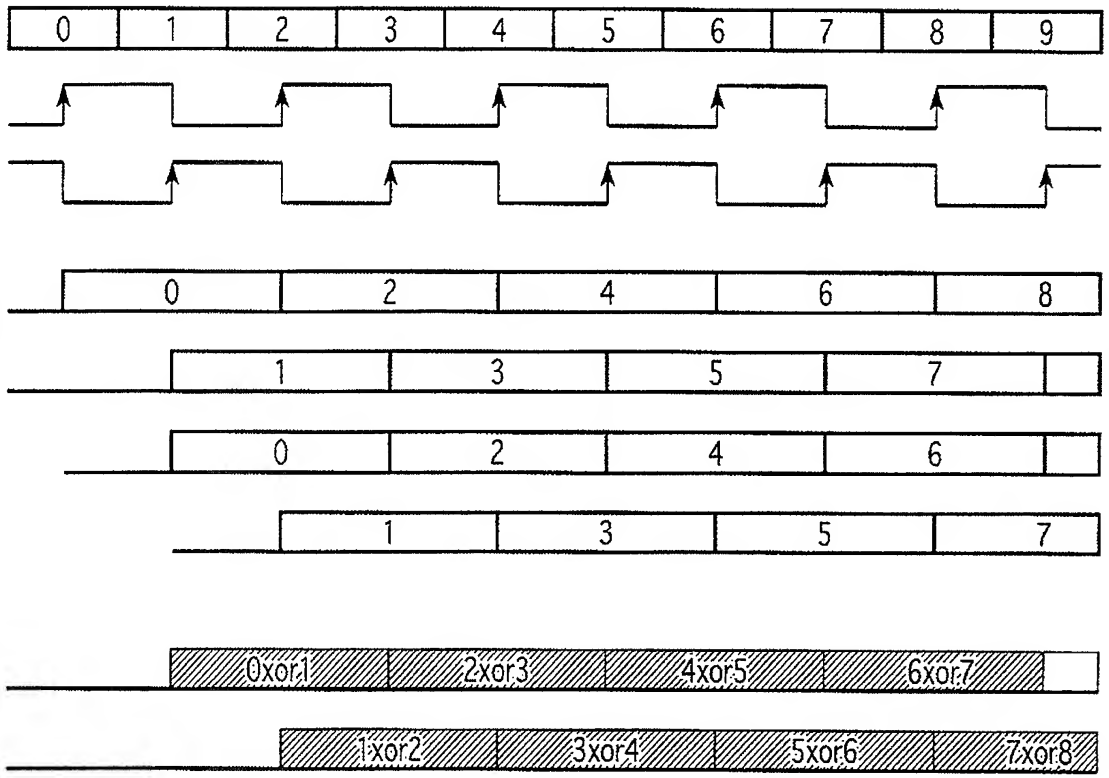

FIG.3 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	
q2	↑ CK2	
q3	↑ CK2	
q4	↑ CK1	
Error1	q2 xor q3	
Error2	q1 xor q4	

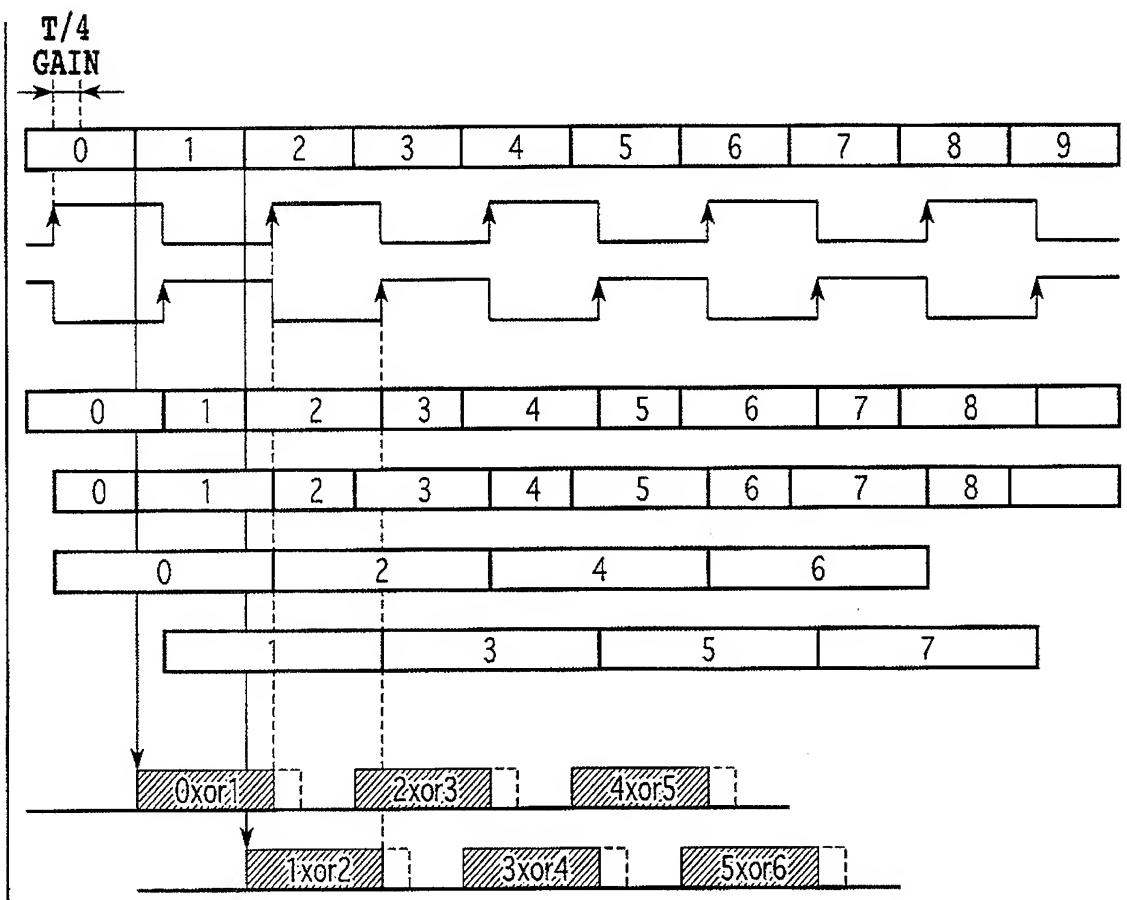

FIG.4 HOLMQVIST AND SUMMERS

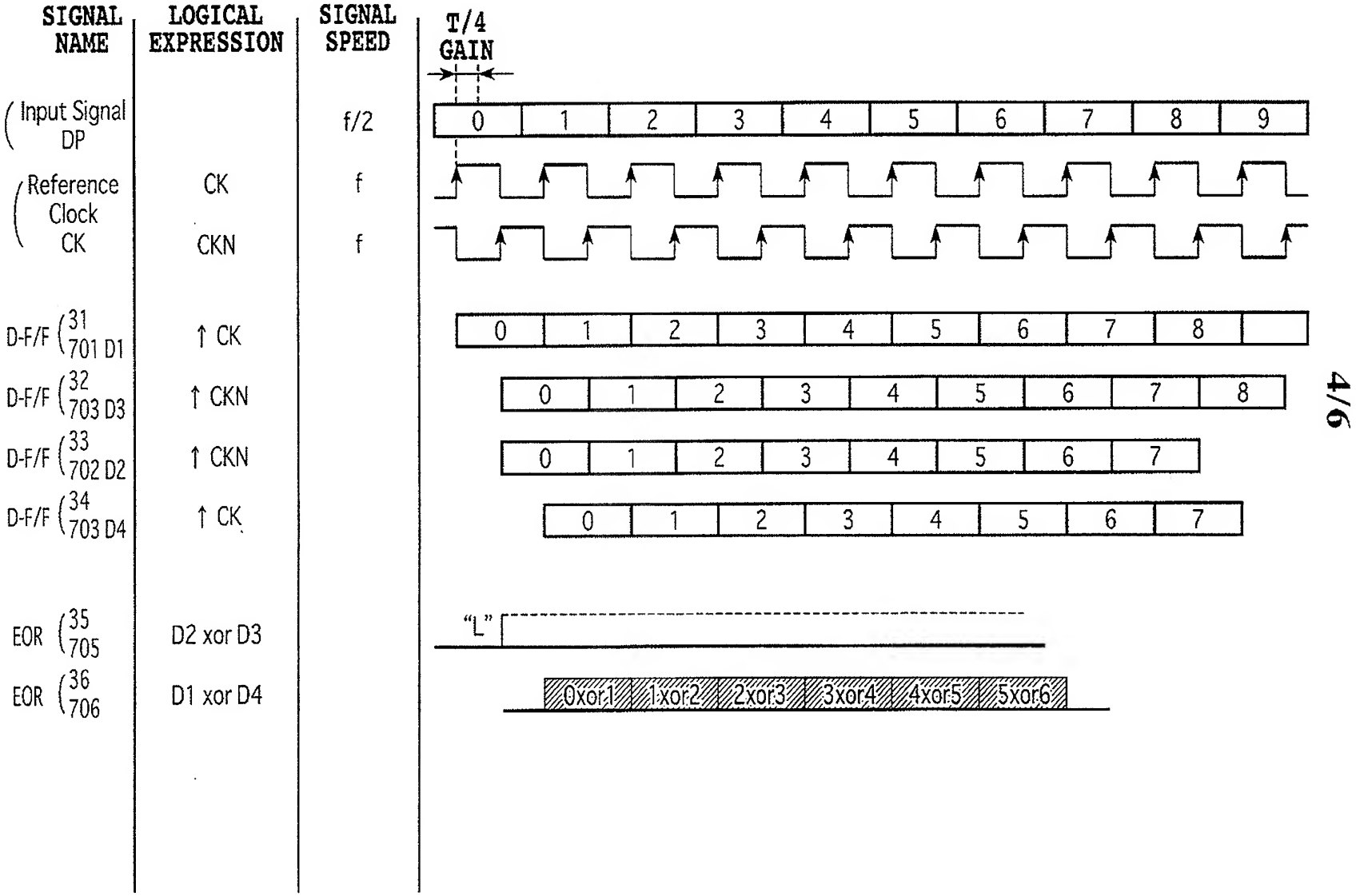

FIG.5 THE PRESENT INVENTION

SIGNAL NAME	LOGICAL EXPRESSION	SIGNAL SPEED
Din		f/2
CK1	CK	f/2
CK2	CKN	f/2
q1	↑ CK1	
q2	↑ CK2	
q3	↑ CK2	
q4	↑ CK1	
Error1	q2 xor q3	
Error2	q1 xor q4	

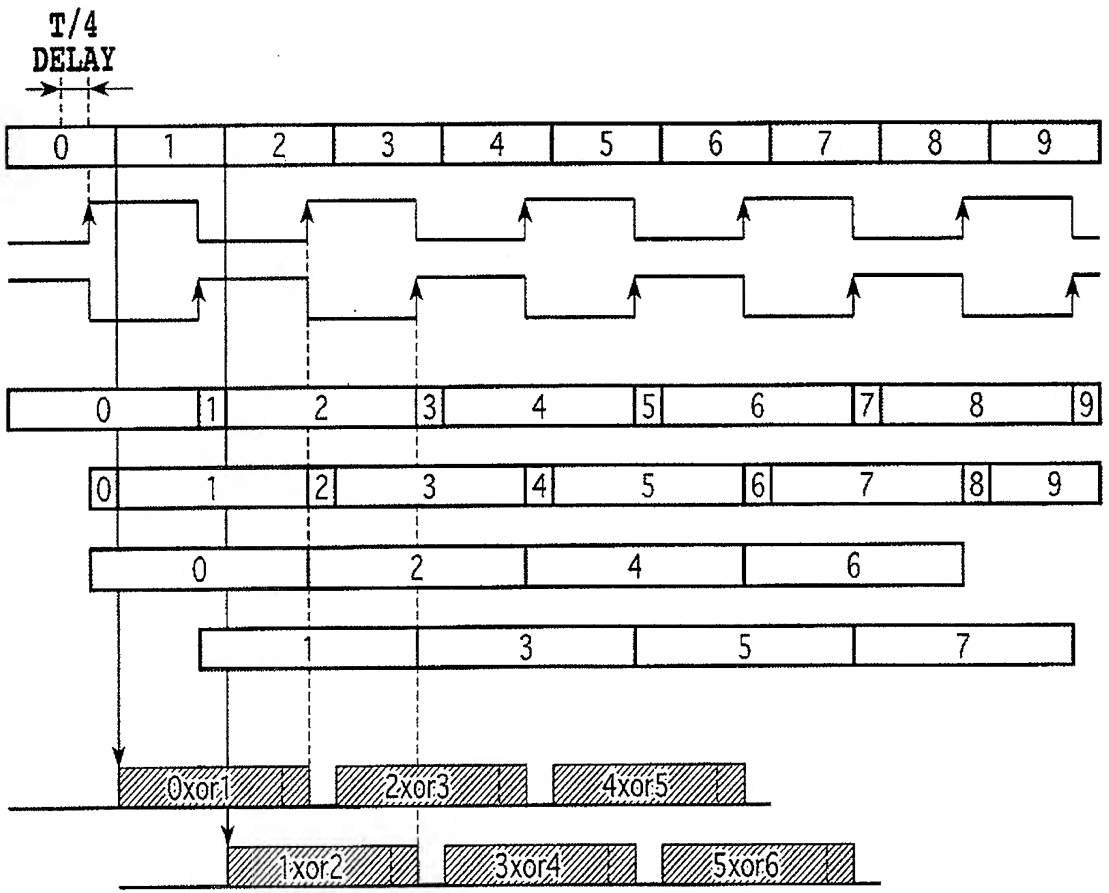
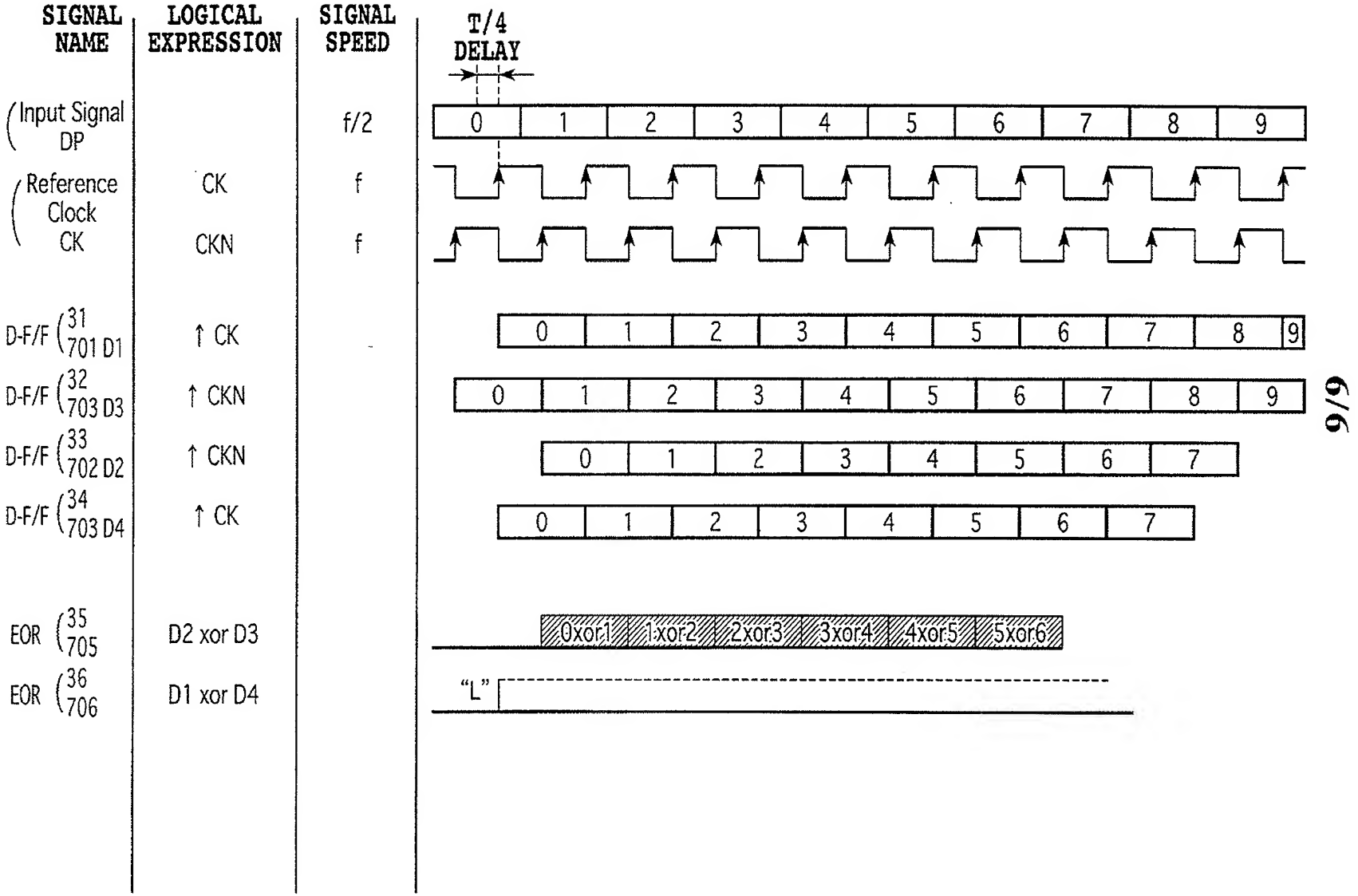
FIG.6 HOLMQVIST AND SUMMERS